Remarks

Claims 1-6 are pending in this action. Claims 1-6 stand rejected. By this amendment claims 1, 2, and 4 have been amended. Applicants respectfully request reconsideration of all pending claims herein.

Applicants respectfully submit that the amendments to claims 1,2, and 4 more clearly define and claim Applicants' invention and distinguish it over the prior art of record. No new matter has been added to the application by virtue of the present amendment.

Claim Rejections - 35 U.S.C. § 102(b)

The Office Action stated that claims 1-6 stand rejected under 35 USC §102(b) as being anticipated by Fujisawa et al. (U.S. Patent Publication No. 2004/0004890). Specifically, regarding claims 1 and 4 the Office Action stated that Fujisawa et al. discloses a semiconductor memory and its corresponding burst operation method for the semiconductor memory.

Applicants have amended claims 1 and 4 to clarify that Applicant's described latches are separate elements connected between the secondary sense amplifiers (SSA) and write buffers (WB), and the I/O bus (see Applicants figs. 2 and 3 PFPLL, and pg. 11-12 paragraphs 0055-57 and 62-63). Claim 1 as amended now recites in part, "… a plurality of prefetch/preload latch circuits (PFPLL) connected in common to each of said data I/O buses, wherein there are a predetermined number of PFPLL for each data I/O bus respectively;

a half of a data path circuit corresponding to a single array block (BK1);

the half of a data path circuit further comprising a plurality of secondary sense amplifiers (SSA), a plurality of write buffers (WB), and the PFPLL, wherein

each secondary sense amplifier supplies read data from the memory to the corresponding PFPLL;

each write buffer supplies write data received from the data I/O bus to the corresponding PFPLL, wherein the PFPLL temporarily retain the read or write data…"

The output circuit of Fujisawa shows/describes buffers connected directly to I/O lines, which are further connected to the main sense amplifiers and not secondary sense amplifiers (Fujisawa Fig. 1 output circuit 18, paragraphs 0046-0047). Therefore, Fujisawa does not anticipate Applicant's claim 1. For the reasons stated above, the latch circuits recited in claim 4 are also not anticipated by Fujisawa. Therefore claims 1 and 4 should pass to issuance.

Accordingly, Applicants respectfully submit that the rejection of claims 1 and 4 under 35 U.S.C. § 102(b) has been overcome. Since Claims 2-3 depend from Claim 1 and Claims 5-6 depend from Claim 4, all claims are in condition for allowance.

Conclusion

Please do not hesitate to call/email the undersigned at the number/email address listed below if there are further questions. Applicants would also be amendable to an Examiner's amendment for the purposes of furthering prosecution.

Respectfully submitted,
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